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APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/040,460	01/09/2002	Terumasa Kitahara	024016-00022	2564

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ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
1050 Connecticut Avenue, N.W., Suite 600
Washington, DC 20036-5339

EXAMINER	
NGUYEN, THINH T	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/040,460	KITAHARA ET AL.	
	Examiner	Art Unit	
	Thinh T Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED OFFICE ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed (see MPEP paragraph 606.01).

A title such as -- Semiconductor integrated circuit device with enhanced layout -- is suggested.

2. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant cooperation is requested In correcting any errors of which the applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

3. The following is a quotation of U.S.C. 103(a) which form the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (fig. 24,25,26,27,28) in view of Yin (US patent 5635737)

and in view of further remark.

REGARDING CLAIM 1.

Applicant Admitted Prior Art disclose all the invention except for the teaching of a Region with no unit wirings; However, Lin (fig 3, region 250, the abstract) teaches the formation of a area with no unit wiring on the CMOS VLSI integrated circuit chip with the focus on the symmetric nature of CMOS device to reduce wiring complexity.

It would have been obvious to one of ordinary skill in the art the time the invention was made to combine the teachings of the AAPA and Yin in order to fabricate

A semiconductor integrated circuit device comprising:

a pair of a first power wiring and a second power wiring, the pairs being arranged in one direction, wherein a first region between the first power wiring and the second power wiring; fundamental circuit units constituted by combining one or more PMOS transistors and one or more NMOS transistors, the fundamental circuit units being arranged along with the first power wiring and the second power wiring; logic circuit units constituted by a plurality of the fundamental circuit units; functional circuit units constituted by a plurality of the logic circuit units, the functional circuit units being connected each other; wherein at least one part of the PMOS transistors and that of the NMOS transistors are arranged below the first power wiring and the second power wiring; and unit connection wirings to connect between the fundamental circuit units or to connect between the logic circuit units, of which terminals terminate at the functional circuit units are arranged on second regions that are other than the first region, in case the unit connection wirings are constituted by a layer that is same as a

wiring layer that constitutes the first power wiring and the second power wiring or by wiring layers that are under the wiring layer of the first and second power wirings.

The rationale to combine the teachings of the AAPA with the teachings of Yin is as follows:

A person of ordinary skill in the art at the time the invention was made would have been motivated to improve the AAPA using the teachings of Yin in order to use less silicon area as suggested by Yin in the abstract.

REGARDING CLAIMS 2-19

The combination of the AAPA and Yin disclose all the invention except for the details of wiring connections, number of PMOS and NMOS transistors per unit cells, the arrangement of wiring units etc...; however, these are mere rearrangement of parts of the combined teachings of the AAPA and Yin for chip size optimization in CMOS technology and are considered routine obvious skill at the time the invention was made for a person of ordinary skill in the art.

5. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and the page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

6. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to be abandoned (see M.P.E.P. 710.02(b)).

7. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d) which papers have been placed of record in the file.

CONCLUSION

8. The prior arts made of record and not relied upon are considered pertinent to applicant disclosure: Saika (US patent 5995734) disclose a method for generating transistor placement in an automatic cell layout design; Okamoto (US patent 6335640) disclose a semiconductor integrated circuit device with its layout design by the cell base method; Tseng et al. (UK Patent Application GB 2300893 A) disclose a flexible CMOS wiring layout method.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose phone number is (703) 305-0421. The Examiner can normally be reached on Monday to Friday from 8.30 A.M. to 5.00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, David C. Nelms can be reached on (703) 308-4910. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Thinh T. Nguyen TTN

Art Unit 2818

HOAI HC
PRIMARY EXAMINER